Understanding RF & Microwave Solid State Switches

Application Note

AN101 – October 2014

Contents

1 General

1.1 Terminology / Abbreviations / Symbols

FET	Field-Effect Transistor
NA	Not Applicable
RF	Radio Frequency
TBD	To Be Decided or To Be Defined

2 Introduction

The RF & Microwave Solid State Switches has the following advantages over mechanical switches; long operating life, fast switching time, low power consumption and small size. Mechanical RF & Microwave Switches usually have lower *insertion loss*, higher *isolation* and higher RF power handling capability. RF & Microwave Solid State Switches are to prefer if very low *insertion loss* or/and very high *isolation* are not needed.

Ranatec Instrument offers a wide range of RF & Microwave Solid State Switches for a wide range of applications such as instrumentation, wireless communication, radar, test systems, etc.

3 RF & Microwave Solid State Switches Overview

3.1 FET switches

In FET switches are Field-Effect Transistors used as the switching elements. The FET types used are usually GaAs, Si-On-Insulator (SOI) or Si-On-Sapphire (SOS). The most common switch configurations are:

- Single-Pole-Single-Throw (SPST) switch route signals from one input to one output, i.e. it connect or disconnect a signal.
- Single-Pole-Double-Throw (SPDT) switch route signals from one input to one of two outputs.
- Single-Pole-Multiple-Throw (SPnT where n ≥ 3) switch route signals from one input to one of multiple outputs.
- Transfer or Double-Pole-Double-Throw (DPDT) switch, see fig. 3.1.1 (a).
- Bypass switch, see fig. 3.1.1 (b).

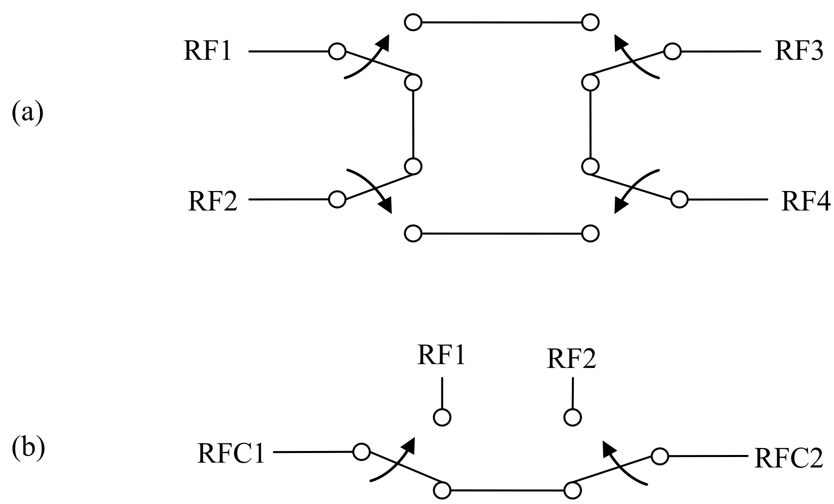

Fig. 3.1.1 (a) is a Transfer switch. The two states are RF1 connected to RF2 and RF3 connected to RF4, or, RF1 connected to RF3 and RF2 connected to RF4. (b) is a Bypass switch.

The switches can be absorptive or reflective. Figure 3.1.2 shows a SPDT of reflective and absorptive type.

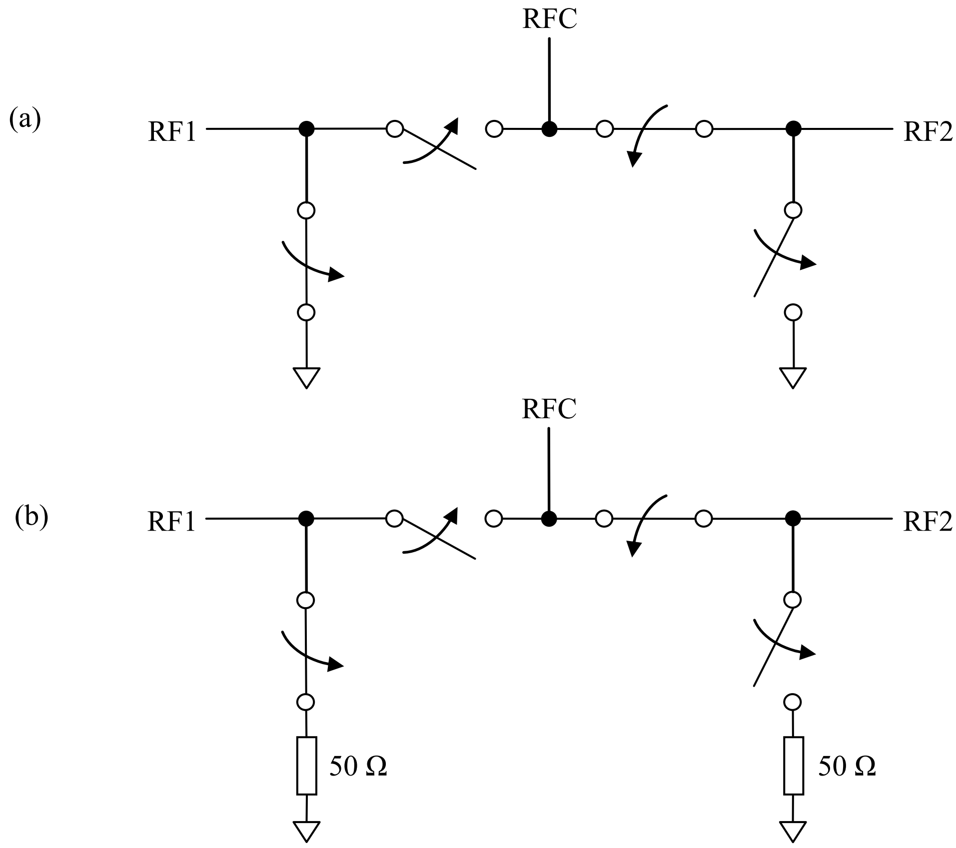

Fig. 3.1.2 (a) is a SPDT of reflective type and (b) is a SPDT of absorptive type. The pole RFC is connected to either RF1 or RF2.

The reflective switch in fig. 3.1.2 (a) has RF2 connected to RFC and, RF1 disconnected from RFC and shorted to signal ground. This means that most of the power of a wave incident to RF1 will be reflected back due to the impedance mismatch between the switch and the transmission line connected to RF1. The absorptive in fig. 3.1.2 (b) has RF2 connected to RFC and, RF1 disconnected from RFC and terminated with 50 ohm (located internally in the switch). This means that most of the power of a wave incident to RF1 will be absorbed in the 50 ohm resistor due to the impedance match between the switch and the transmission line connected to RF1.

The FET as a switching element suffers from non-ideal properties, like most other types of switching elements. In its low impedance state, the resistance R_{dson} between drain and source of the FET switch is not zero ohm. This gives a power loss in the FET when a signal passes through the FET. This is associated with the switch parameter ***Insertion Loss***. The *Insertion Loss* at FET switches are very repeatable, so it can be calibrated and compensated for, when signal levels need to be known with high accuracy.

A fraction of the signal power leak through parasitic capacitances in the FET when in the high impedance state (OFF state). This gives a limited isolation when the switch is in its OFF state. This is associated with the switch parameter ***isolation***.

R_{dson} not being zero in conjunction with parasitic capacitances in the FET, give rise to a reflection of a fraction of an incident wave to RFC or RF2 in fig. 3.1.2, even if RFC or RF2 is terminated with an ideal 50 ohm termination. This is associated with the switch parameter ***VSWR RFC-RFx*** or ***Return Loss RFC-RFx***.

R_{dson} not being zero in conjunction with parasitic capacitances in the FET and non-ideal internal 50 ohm termination, give rise to a reflection of a fraction of an incident wave to RF1 in fig. 3.1.2 (b). This is associated with the switch parameter ***VSWR terminated port*** or ***Return Loss terminated port***.

The FET is a non-linear switch element, which generate intermodulation and harmonic distortion. The switch parameter ***Input* 1 *dB compression*** or ***P1dB*** is the input power at which the *Insertion Loss* has increased with 1 dB relative the insertion loss at low input power levels. The parameter ***Input* 1 *dB compression*** or ***P1dB*** is an indication of how non-linear the switch is. The higher P1dB, the less non-linear. But it's just an indication, a better metric for non-linearity is the switch parameters ***Input IP*2** and ***Input IP*3**. IP2 and IP3 (intercept point of second and third order) are usually measured by letting two tones with equal amplitude, at frequency f_1 and f_2, pass through the device under test. Distortion products are then generated at frequencies f_{nm} as follows

$$f_{nm} = \left| \pm nf_1 \pm mf_2 \right|, \; n, m \in \{0,1,2,...\} \tag{3.1.1}$$

and the *order* of the distortion product is

$$order = n + m \tag{3.1.2}$$

When n or m is zero, then is f_{nm} the frequencies of the harmonics, otherwise is f_{nm} the frequencies of the intermodulation products. In many cases are only second and third order distortion products significant in amplitude, the higher order distortion products decay rapidly as the order increase. Figure 3.1.3 shows the frequency locations of second and third order distortion products.

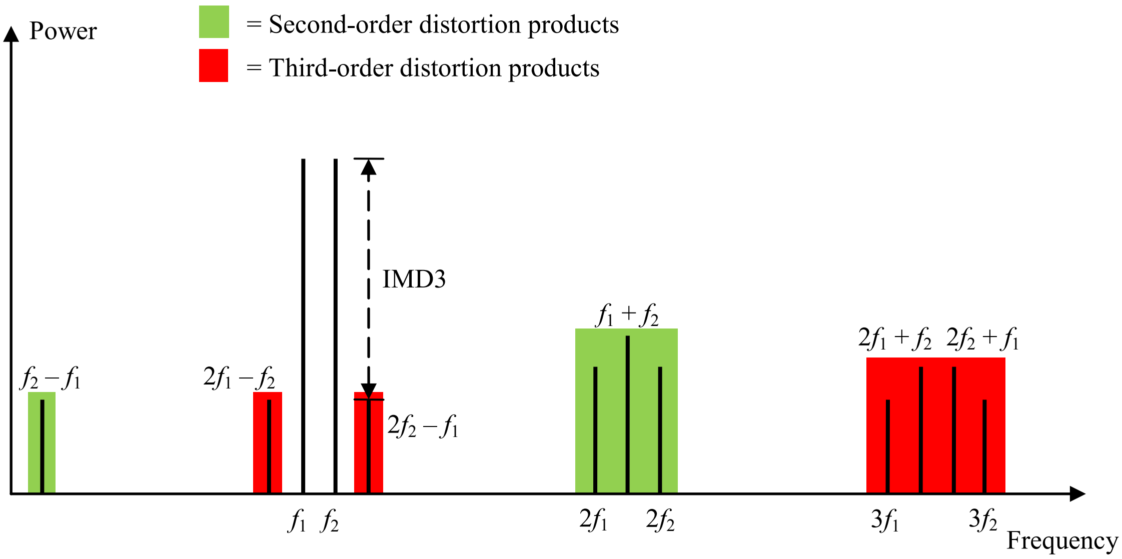

Fig. 3.1.3 Second and third order distortion products when two tones, at frequency f_1 and f_2, with equal amplitude pass through a non-linear device.

In many cases are only the third-order products at $2f_1 - f_2$ and $2f_2 - f_1$ of interest, because signals through the device usually have narrow bandwidth and is band-pass filtered at some receiving unit. The power P_3 in dBm of one of the tones at the frequency $2f_1 - f_2$ or $2f_2 - f_1$ can be calculated as follows

$$P_3 = 3P_{in} - 2IP_3 \qquad (3.1.3)$$

where

P_{in} = the input power in dBm of one of the two tones, with equal amplitude, at f_1 or f_2.

IP_3 = the third order intercept point, related to the input, in dBm.

The FET switch has a limited power handling capability. This is specified with the switch parameters, ***max power thru path***, ***max power hot switching*** and ***max power into termination***. The *max power thru path* is the maximum input power to RFC or RFx when they are connected (see fig. 3.1.2) and source and load impedance is 50 ohm. The *max power hot switching* is the maximum input power to RFC (see fig. 3.1.2) when RFC is switched to different RFx with the input power present during the switching and, source and load impedance is 50 ohm. The *max power into termination* is the maximum input power to RFx when RFx is terminated to the internal 50 ohm (see RF1 in fig. 3.1.2 (b)).

The switch parameters ***Switching Time*** and ***Settling Time*** specify how fast the switch can change the route of a signal. These two parameters are defined in fig. 3.1.4.

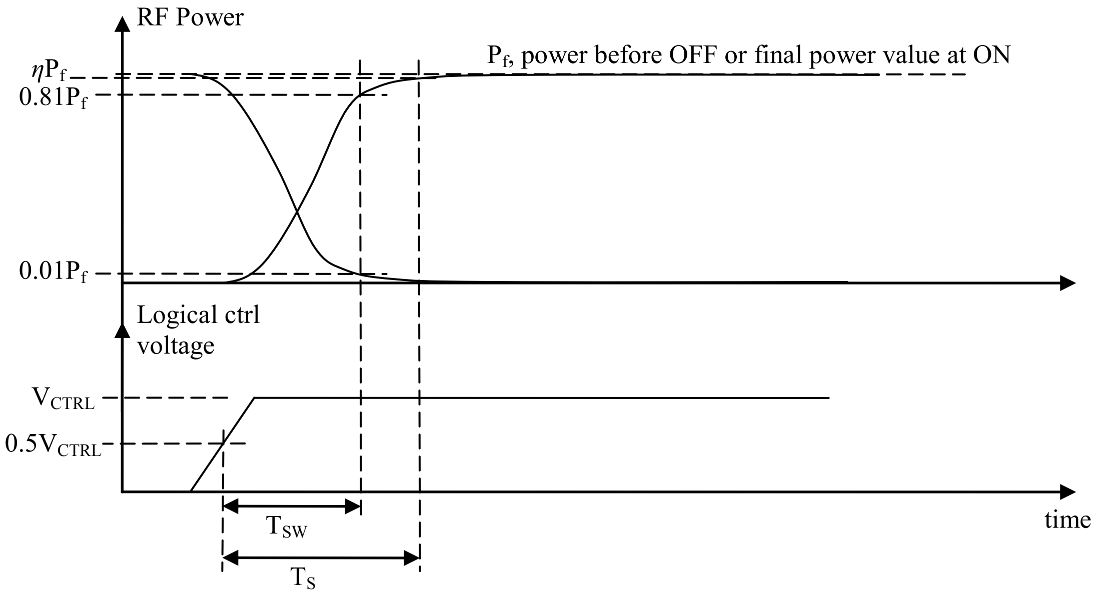

Fig. 3.1.4 The switching time T_{SW} and settling time T_S. The $0.81P_f$ level corresponds to the 90 % voltage level and $0.01P_f$ level corresponds to the 10 % voltage level and ηP_f ($\eta < 1$) is the level where the RF power is assumed to be settled, and this level is chosen by the manufacturer. The logical control voltage is the logical signal that controls the switching.

3.2 PIN diode switches

An RF/microwave PIN diode is a semiconductor device that operates as a variable resistor at RF/microwave frequencies. The resistance at RF/microwave frequencies is controlled with the DC current through the PIN diode. The higher DC current through the PIN diode, the lower RF/microwave resistance. It's the variable resistor property that makes it possible to use PIN diodes in switch and variable attenuator designs.

The PIN diode has a high resistivity intrinsic I region in-between the P-type and N-type region of the diode as shown in fig. 3.2.1.

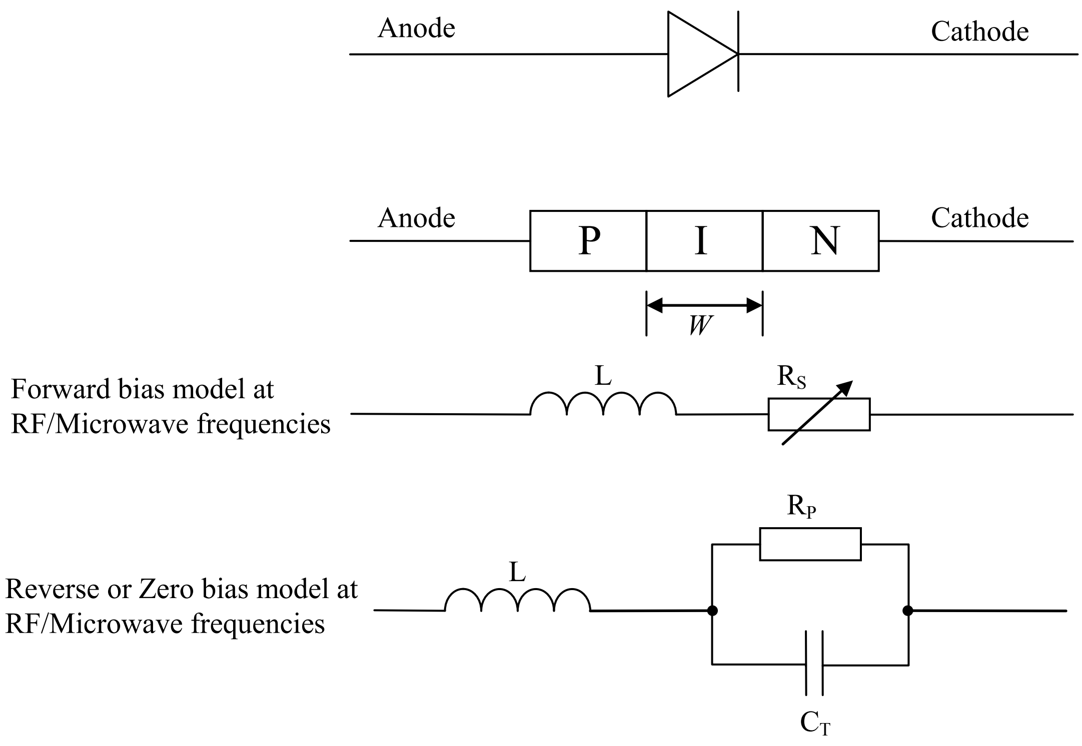

Fig. 3.2.1 The PIN diode structure and models.

Holes and electrons enters the I region when the PIN diode is forward biased, and there they recombine, but not immediately. The average time it takes to recombine is called the carrier lifetime τ. This means that an average charge Q is stored in the I region, which lowers the resistance of the I region to some value R_S. The average stored charge Q when the PIN diode is forward biased with the current I_F is

$$Q = I_F \tau \tag{3.2.1}$$

and the resistance R_S of the I region is

$$R_S = \frac{W^2}{(\mu_N + \mu_P)Q} \qquad (3.2.2)$$

where

W = the I region width, see fig. 3.2.1

μ_N = the electron mobility

μ_P = the hole mobility

By combining equ. (3.2.1) and (3.2.2) is the following obtained

$$R_S = \frac{W^2}{\tau(\mu_N + \mu_P)I_F} \qquad (3.2.3)$$

From equ. (3.2.3) we see that R_S is inversely proportional to I_F. One can argue that a normal PN diode has an AC resistance that is the derivative dV/dI of the V-I characteristic of the diode. The derivative dV/dI of a PN diode decrease with increased DC bias current, i.e. the AC resistance decrease with increased DC bias current. So why use a PIN diode when a normal PN diode can be used instead. The AC resistance (at RF/microwave frequencies) of a PIN diode is very linear, but the AC resistance of a normal PN diode is highly non-linear. The current through a normal PN diode follows the curvature of the V-I characteristic which gives a non-linear AC resistance, but the resistance of the PIN diode is the resistance of the I region. Non-linearities give rise to distortion products, see fig. 3.1.3. A PIN diode has a lower frequency limit for equ. (3.2.3) to be valid. The PIN diode characteristics are similar to a PN diode when operated under this frequency limit. This frequency limit is called the transit time frequency f_T and is expressed as

$$f_T = \frac{1300}{W^2} \text{ [MHz]} \qquad (3.2.4)$$

where

W = the I region width in µm

Two types of simple SPST PIN diode switches can be seen in fig. 3.2.2.

A FET switch can be made to have the lower frequency limit at DC, but this is not possible for a PIN diode switch (see equ. (3.2.4)). The power consumption of a PIN diode switch is much higher than the power consumption of a FET switch, that is because the need of a bias current through the PIN diodes. PIN diode switches have much higher video leakage than FET switches. ***Video leakage*** is when parts of the control signal leaks out to the RF port. The control signal of a PIN diode switch is the PIN diode bias current which pass through the RF signal path also (see 3.2.2), and can thereby generate spurious signals at the load connected to the RF path. This phenomenon is more pronounced if the switch needs to be fast regarding switching time and the control signal has short rise and fall time. The frequency spectrum upper frequency limit of the video leakage can reach to over 100 MHz. But a FET switch is controlled with a control voltage at the gates of the FET transistors and the gates are not a part of the RF signal path, so the *Video Leakage* is much less in a FET switch.

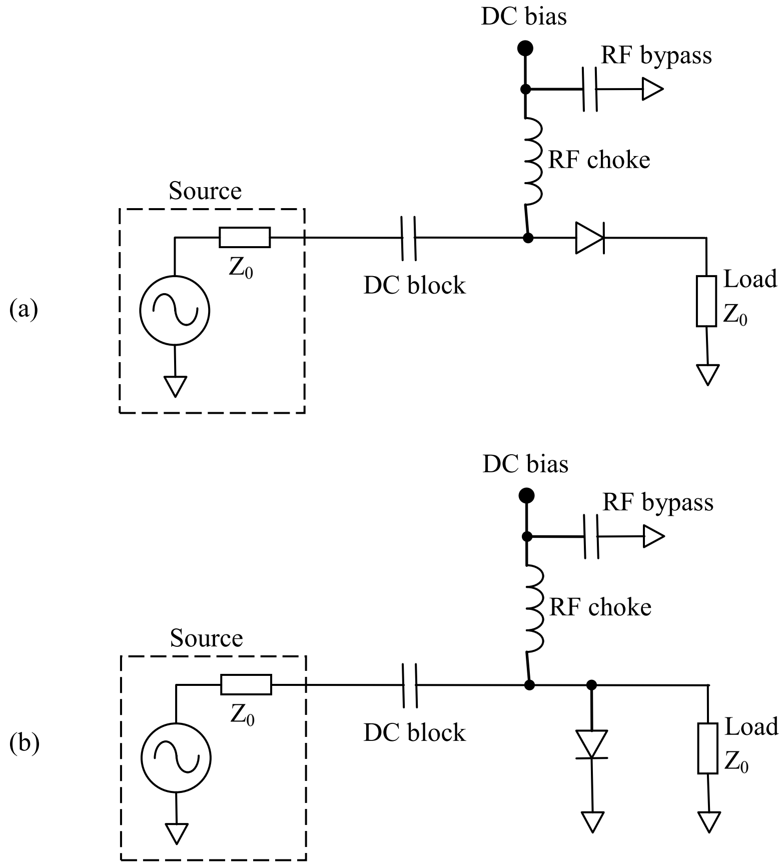

Fig. 3.2.2 (a) SPST series PIN diode switch. (b) SPST shunt PIN diode switch. Both switches are of reflective type.

4 RF & Microwave Solid State Switch Parameters

Insertion Loss or ***IL*** is the relative power loss of the connected path of the switch, i.e. IL = $10\log(P_{in}/P_{out})$ [dB].

Isolation is the relative power loss of a disconnected path of the switch, i.e. Isolation = $10\log(P_{in}/P_{out})$ [dB].

VSWR RFC-RFx or ***Return Loss RFC-RFx*** is the VSWR or Return Loss of an incident wave to RFC or RFx when RFC and RFx are connected via the switch and, both ports are source/load terminated with an ideal 50 ohm termination.

VSWR terminated port or ***Return Loss terminated port*** is the VSWR or Return Loss of an incident wave to RFx when RFx is disconnected from RFC, see RF1 in fig. 3.1.2 (b).

Input* 1 *dB compression or ***P*1*dB*** is the input power at which the *Insertion Loss* has increased with 1 dB relative the insertion loss at low input power levels. The *P*1*dB* level may be higher than the *Max power thru path* level, if so, the switch can't be operated at the *P*1*dB* level.

***Input IP*2** and ***Input IP*3** is the intercept point of second and third order. See section 3.1, equ. (3.1.1) to (3.1.3) and fig. 3.1.3.

Max power thru path is the maximum input power to RFC or RFx when they are connected via the switch (see fig. 3.1.2) and source and load impedance is 50 ohm.

Max power hot switching is the maximum input power to RFC (see fig. 3.1.2) when RFC is switched to different RFx with the input power present during the switching and, source and load impedance is 50 ohm.

Max power into termination is the maximum input power to RFx when RFx is terminated to the internal 50 ohm (see RF1 in fig. 3.1.2 (b)).

Switching Time and ***Settling Time*** is defined in fig. 3.1.4.

Video leakage is when parts of the control signal leaks out to the RF port, usually specified in the unit mV_{pp}. The video leakage presents itself, during and a short time after, the rising or falling edge of the control signal. The video leakage signal usually looks like a ringing signal with short duration. The specified video leakage is the peak-to-peak voltage of the ringing signal at the RF port.

Revision Changes

Rev.	Date	Change	Reference	Approved
1.0	2014-10-16	First revision.	Jan Dahl	Tomas Ornstein